REMARKS

The present response is intended to be fully responsive to all points of objection and/or rejection raised by the Examiner and is believed to place the application in condition for allowance. Favorable reconsideration and allowance of the application is respectfully requested.

Applicants assert that the present invention is new, non-obvious and useful. Prompt consideration and allowance of the claims is respectfully requested.

Status of Claims

Claims 1 through 17 are pending in the application. Claims 7 through 9 and 13 have been objected to. Claims 1 through 6, 10 through 12 and 14 through 17 have been rejected.

Allowable Subject Matter

In the Office Action, the Examiner stated that claims 7 through 9 and 13 would be allowable if rewritten in independent form.

CLAIM REJECTIONS

35 U.S.C. § 102 Rejections

In the Office Action, the Examiner rejected claims 1 through 6, 8 through 12 and 15 through 17 under 35 U.S.C. § 102(e), as being anticipated by U.S. Pat. No. 6,967,872 B2 to Quader et al. (the '872 patent). Applicants respectfully traverse this rejection in view of the remarks that follow.

Independent claims 1 and 15 in the present application recite:

> *1. A multi-phase method of programming an array of non-volatile memory ("NVM") cells, said method comprising:*
>
> *Applying to a first set of NVM cells first phase programming pulses; and*
>
> *upon one or more NVM cells of the first set of cells reaching or exceeding a first intermediate threshold voltage level, applying to a terminal of two or more cells in*

the first set of cells second phase programming pulses adapted to induce relatively greater threshold voltage changes in cells having less stored charge than in cells having relatively more stored charge.

15. A System for programming an array of non-volatile memory ("NVM") cells, said system comprising:

a controller adapted to cause a charge circuit to produce first phase programming pulses and to determine when one or more NVM cell of a first set of cells receiving the first phase programming pulses reaches or exceeds a first intermediate voltage, and to then cause said charge pump circuit to ***apply to a terminal the one or more cells in the first set second phase programming pulses adapted to induce relatively greater threshold voltage changes in cells having less stored charge than in cells having relatively more stored charge.***

The '872 patent teaches:

> **"A multi-level non-volatile memory cell programming/lockout method and system are provided. The programming/lockout method and system advantageously prevent memory cells that charge faster than other memory cells from being over-programmed. "** ('872 patent abstract)

In the Office Action, the Examiner had stated that "Fig 7 of Quarter discloses a multi-phase method of programming an array of non-volatile memory ("NVM") cells..."

The '872 patent teaches:

> **"...FIG. 7 illustrates one embodiment of a method of programming, verifying and locking out a plurality of memory cells in the memory array 1 of FIG. 1 or the memory array 311 in FIG. 3. In a block 700 of FIG. 7, the controller 20 in FIG. 1 receives a mixed data pattern, which corresponds to multiple states such as Vt0, Vt1, Vt2 and Vt3, to be written to one or more pages of memory cells in the memory array 1. The system 100 (FIG. 1) inhibits programming of all memory cells selected to be in a Vt0 state in the memory page(s). The system 100 simultaneously programs all memory cells selected to store Vt1 data, all memory**

cells selected to store Vt2 data and all memory cells selected to store Vt3 data with programming pulses in a block 700." ('872 patent detailed description)

The '872 teaches "Lockout Method(s)", such as the one cited hereinabove in Fig.7, that handle the problem of fast bits and slow bits. The '872 patent introduces the problem of fast bits and slow in the following way:

"The programming method described above is acceptable if the threshold voltage levels of the memory cells increase in parallel without too many "fast bits" or "slow bits," which are memory cells with floating gates that experience a fast or slow increase in charge and threshold voltage levels. Fast bits and slow bits may be caused by a number of factors, such as variations or imperfections in transistor fabrication, altered transistor properties due to repeated programming and erasing, etc. If there is a significant number of fast bits and/or slow bits, then the preceding method may result in over-programmed or under-programmed memory cells..."

In general, a "Lockout Method" is characterized by inhibiting the programming of memory cells that reached a certain threshold, programming the cells that hadn't reached that threshold, these steps are repeated until all the cells had reached that threshold. Citing from the '872 patent claim no.1:

"...inhibiting programming of any memory cell that has reached or exceeded the first predetermined threshold voltage level.."

Although the cited '872 teaches the programming of NVM cells using multiple series of programming pulses, and shows different methods for overcoming the problem of fast bits and slow bits, the '872 patent neither teaches nor suggests that a second series of pulses would "**induce relatively greater threshold voltage changes in cells having less stored charge than in cells having relatively more stored charge.**" This limitation in present in both independent claim 1 and 15, but neither taught nor suggested in the '872 patent. Therefore, neither of these claims are anticipated by the '872 patent.

Applicants respectfully request reconsideration and withdrawal of the rejections of claims 1 and 15. Since claims 2 through 14 depend from claim 1, and claim 16 through 17

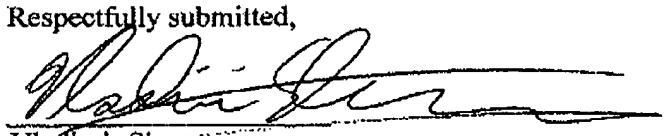
depend from claim 15, Applicants consider claims 2 through 14 and claims 16 through 17 to be allowable by virtue of their dependence on allowable base claims.

Applicants consider the above explanation to render the 103 rejection of claim 14 moot.

In view of the foregoing amendments and remarks, the pending claims are deemed to be allowable. Their favorable reconsideration and allowance is respectfully requested.

Should the Examiner have any question or comment as to the form, content or entry of this Amendment, the Examiner is requested to contact the undersigned at the telephone number below. Similarly, if there are any further issues yet to be resolved to advance the prosecution of this application to issue, the Examiner is requested to telephone the undersigned counsel.

Respectfully submitted,



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